LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a die having formed therein a semiconductor switching device and a schottky device,

said semiconductor switching device including a plurality of gate trenches each including a pair of opposing sidewalls and a bottom wall and each extending from a top surface of said die to a drift region in the body of said die, channel regions of a first conductivity type formed in said die and disposed adjacent the sidewalls of said gate trenches, a gate insulation layer disposed on each sidewall of a gate trench adjacent a respective channel region, conductive gate material contained within said gate trenches and insulated from said channel regions by said gate insulation layers, and regions of a second conductivity type opposite to the conductivity type of said channel region each disposed at a sidewall of a respective gate trench and each extending from the top surface of said die to a respective channel region;

said schottky device including a schottky barrier disposed over and in schottky contact with a portion of the top surface of said die;

a first contact in contact with said schottky barrier and said regions of said second conductivity type; and

a termination structure, said termination structure being comprised of a depression formed in said die to a depth below that of said channel region, a first insulation layer formed over major surfaces of said depression, a conductive layer formed over said insulation layer, a second insulation layer formed over said conductive layer, and a termination contact formed over said second insulation layer, wherein said termination contact is in electrical contact with said conductive layer through said second insulation layer.

2. (Original) A semiconductor device according to claim 1, further comprising a second contact in contact with a major surface of said die opposite said first contact.

3. (Original) A semiconductor device according to claim 1, wherein said semiconductor switching device is a MOSFET.

4. (Original) A semiconductor device according to claim 1, wherein said schottky barrier comprises $TiSi_2$.

5. (Original) A semiconductor device according to claim 1, wherein said schottky barrier is disposed over a major surface of a mesa formed in said die.

6. (Currently Amended) A semiconductor device according to claim 1, wherein said schottky device further comprises a mesa having a schottky trench formed on either side thereof, each schottky trench having an insulation layer formed on its side walls and bottom and containing a conductive material.

7. (Currently Amended) A semiconductor device according to claim 6, wherein said schottky barrier extends over said sidewalls of said schottky trenches.

8. (Original) A semiconductor device according to claim 1, further comprising a high conductivity region of the same conductivity as said channel region disposed between each pair of said regions of said second conductivity type and in contact with said first contact.

9. (Original) A semiconductor device according to claim 8, wherein said high conductivity region is located at the bottom of a recess in said die.

10. (Currently Amended) A semiconductor device according to claim 1, wherein each of said gate trenches includes a thick oxide layer at the bottom thereof.

Claims 11 - 17 (Cancelled).

18. (Currently Amended) A semiconductor device comprising:

a die having formed therein a schottky device and a MOS-gated switching device, said schottky device including a plurality of schottky regions formed on a surface of said die, and said MOS-gated switching device including a channel region, and a plurality of gate structures, each structure including a gate trench having an insulation layer formed on its sidewalls and containing a conductive electrode; and a termination structure, said termination structure being comprised of a depression formed in said die to a depth below that of said channel region, a first insulation layer formed over major surfaces of said depression, a conductive layer formed over said insulation layer, a second insulation layer formed over said conductive layer, and a termination contact formed over said second insulation layer, wherein said termination contact is in electrical contact with said conductive layer through said second insulation layer; and

wherein said gate structures are formed in groups and spaced from one another by a schottky region.

19. (Original) A semiconductor device according to claim 18, wherein said MOS-gated switching device is a MOSFET.

20. (Original) A semiconductor device according to claim 18, wherein each schottky region includes a schottky barrier comprising $TiSi_2$.

21. (Original) A semiconductor device according to claim 20, wherein each schottky barrier is disposed over a major surface of a mesa formed in said die.

22. (Currently Amended) A semiconductor device according to claim 18, wherein each schottky region further comprises a mesa having a schottky trench formed on either side thereof, each schottky trench having an insulation layer formed on its side walls and bottom and containing a conductive material.